IFW

Docket No.: 071971-0015 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Shiro SAKIYAMA, et al.	:	Confirmation Number: CNF NO. 6689
Application No.: 10/511,165	:	Group Art Unit: 2811
Filed: October 14, 2004	:	Examiner: Not yet assigned

For: SEMICONDUCTOR INTEGRATED CIRCUIT

REQUEST FOR CORRECTED FILING RECEIPT

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Sir:

Attached is a copy of the Filing Receipt received from the U.S. Patent and Trademark Office in the above-referenced application. It is noted that the Domestic priority data is incorrect. Attached is a copy of the Front Page of the Published International Application, which evidences that the Domestic Priority data should read: PCT/JP04/01942 02/19/2004. It is requested that a corrected filing receipt be issued.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:blg
Facsimile: 202.756.8087
Date: May 13, 2005

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/511,165	10/14/2004	2811	1250	71971-015	18	16	3

CONFIRMATION NO. 6689

20277
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

FILING RECEIPT

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Date Mailed: 04/08/2005

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Shiro Sakiyama, Yawata-shi, Kyoto, JAPAN;
Masayoshi Kinoshita, Settsu-shi, JAPAN;
Masaya Sumita, Amagasaki-shi, JAPAN;

Power of Attorney: The patent practitioners associated with Customer Number **20277**.

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP04/01942 02/19/2003

Foreign Applications

JAPAN 2003-047418 02/25/2003

Projected Publication Date: To Be Determined - pending completion of Security Review

Non-Publication Request: No

Early Publication Request: No

Title

Semiconductor integrated circuit

Preliminary Class
257

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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(71) 出願人 (米国を除く全ての指定国について): 松下電器産業株式会社 (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) [JP/JP]; 〒5718501 大阪府門真市大字門真１００６番地 Osaka (JP).

(72) 発明者; および

(75) 発明者/出願人 (米国についてのみ): 崎山 史朗 (SAKIYAMA, Shiro). 木下 雅善 (KINOSHITA, Masayoshi). 炭田 昌哉 (SUMITA, Masaya).

(74) 代理人: 前田 弘 , 外 (MAEDA, Hiroshi et al.); 〒5500004 大阪府大阪市西区靭本町１丁目４番８号本町中島ビル Osaka (JP).

(81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

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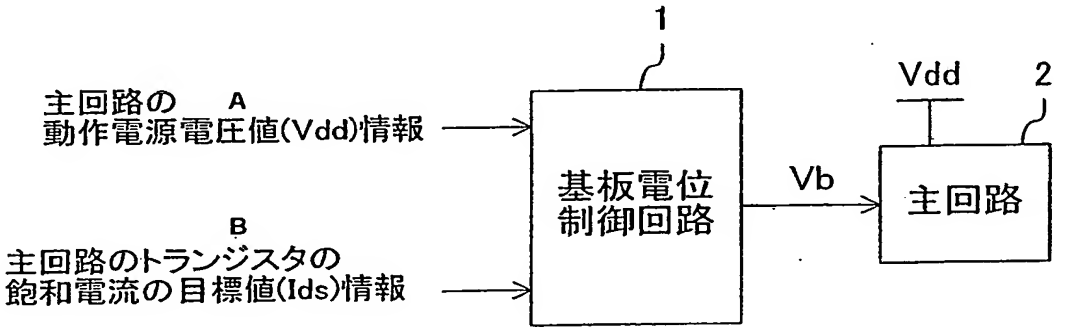
[続葉有]

(54) Title: SEMICONDUCTOR INTEGRATED CIRCUIT

(54) 発明の名称: 半導体集積回路



A...INFORMATION CONCERNING OPERATING POWER SUPPLY VOLTAGE (Vdd) OF MAIN CIRCUIT
B...INFORMATION CONCERNING TARGET SATURATION CURRENT VALUE (Ids) OF TRANSISTOR OF MAIN CIRCUIT
1...SUBSTRATE POTENTIAL CONTROLLING CIRCUIT
2...MAIN CIRCUIT

(57) Abstract: A semiconductor integrated circuit comprises a main circuit (2) which is composed of a MOS transistor wherein a source and a substrate are separated from each other. A substrate potential controlling circuit (1) controls the substrate potential of the MOS transistor of the main circuit (2) so that the actual saturation current value of the MOS transistor which constitutes the main circuit (2) becomes equal to a target saturation current value (Ids) of the main circuit (2) at the operating power supply voltage (Vdd). Consequently, even when the operating power supply voltage of the semiconductor integrated circuit is lowered, variations in the operating speed can be suppressed within a small range.

[続葉有]

WO 2004/077673 A1

MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

添付公開書類:
— 国際調査報告書

２文字コード及び他の略語については、定期発行される各*PCT*ガゼットの巻頭に掲載されている「コードと略語のガイダンスノート」を参照。

(57) 要約: 半導体集積回路において、主回路２は、ソースと基板とが分離されたＭＯＳトランジスタで構成される。基板電位制御回路１は、主回路２を構成するＭＯＳトランジスタの実際飽和電流値が、主回路２の動作電源電圧Ｖｄｄの下での目標飽和電流値Ｉｄｓとなるように、主回路２のＭＯＳトランジスタの基板電位を制御する。従って、半導体集積回路の動作電源電圧が低電圧化しても、動作速度のばらつきを小さく抑制できる。